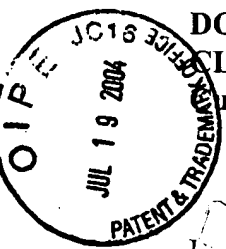


IFW



DOCKET NO.: P05827  
CLIENT NO.: NATI15-05827  
Customer No.: 23990

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of : RICHARD W. FOOTE  
U.S. Serial No. : 10/803,273  
Filed : March 18, 2004  
For : SYSTEM AND METHOD FOR PROVIDING IMPROVED  
TRENCH ISOLATION OF SEMICONDUCTOR DEVICES  
Group No. : 2812  
Examiner : Not Yet Assigned

**MAIL STOP AMENDMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

**CERTIFICATE OF MAILING BY FIRST CLASS MAIL**

The undersigned hereby certifies that the following documents:

1. Postcard receipt;
2. Information Disclosure Statement;
3. Form PTO/SB/08A and PTO/SB/08B; and
4. Eighteen (18) references.

relating to the above application, were deposited as "First Class Mail" with the United States Postal Service, addressed to, MAIL STOP AMENDMENT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 16, 2004.

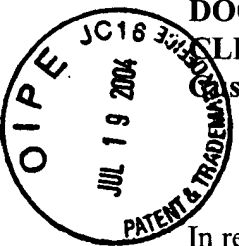
Date: July 16, 2004

Kathleen Newsome  
Mailer

Date: July 16, 2004

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DOCKET NO.: P02709

PATENT

CLIENT NO.: NATI15-05827

Customer No.: 23990

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of : RICHARD W. FOOTE  
U.S. Serial No. : 10/803,273  
Filed : March 18, 2004  
For : SYSTEM AND METHOD FOR PROVIDING IMPROVED  
TRENCH ISOLATION OF SEMICONDUCTOR DEVICES  
Group No. : 2812  
Examiner : Not Yet Assigned

MAIL STOP AMENDMENT  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

**INFORMATION DISCLOSURE STATEMENT**

Pursuant to the duty of disclosure under 37 C.F.R. § 1.56, Applicant submits this statement. This submittal is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure. The patents and publications herein are listed below and on the attached Forms PTO/SB/08A and PTO/SB/08B. Copy of the listed patents and publications are submitted herewith.

<u>U.S. Patent No.</u>	<u>Inventor</u>	<u>Date</u>
4,631,803	Hunter et al.	December 30, 1986
4,835,115	Eklund	May 30, 1989
4,983,226	Hunter et al.	January 8, 1991
5,106,777	Rodder	April 21, 1992
5,358,891	Tsang et al.	October 25, 1994
5,448,102	Gaul et al.	September 5, 1995
5,468,676	Madan	November 21, 1995
5,474,953	Shimizu et al.	December 12, 1995
5,683,908	Miyashita et al.	November 4, 1997
5,872,044	Hemmenway et al.	February 16, 1999
5,874,317	Stolmeijer	February 23, 1999
5,920,108	Hemmenway et al.	July 6, 1999
6,069,057	Wu	May 30, 2000

Publications

Naresh Thapar et al., "Elimination of the "Birds Beak" in Trench MOS-Gate Power Semiconductor Devices", Power Semiconductor Research Center, 1996 IEEE, Pp. 83-86.

G. Fallico et al., "A New Process for Defect-Free Definition of Active Areas in Deep Trench Isolated Bipolar Devices", Microelectronic Engineering 15 (1991) Pp. 655-658.

R. Bashir et al., "PLATOP: A Novel Planarized Trench Isolation and Field Oxide Formation Using Poly-Silicon", IEEE Electron Device Letters, Vol. 17, No. 7, July 1996, Pp. 352-354.

H. Bernhard Pogge, "The Spaces Between the Functions On a Chip", Chemtech, March 1986, Pp. 168-173.


R. Jerome et al., "The Effect of Trench Processing Conditions on Complementary Bipolar Analog Devices with SOI/Trench Isolation", IEEE 1993 Bipolar Circuits and Technology Meeting 3.2, Pp. 41-44.

Applicant hereby expressly reserves the right to swear behind the effective dates of any of the above Patents and to question the relevance and materiality of the Patents and Publications listed herein, in whole, in part, or in combination, subsequent to filing this Information Disclosure Statement.

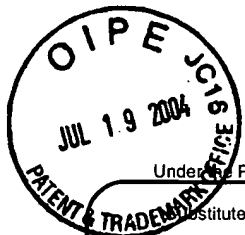
Respectfully submitted,

DAVIS MUNCK, P.C.

Date: July 16, 2004

  
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PTO/SB/08A (08-03)

Approved for use through 07/31/2006. OMB 0651-0031

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Institute for form 1449/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 2

**Complete if Known**

Application Number	10/803,273
Filing Date	March 18, 2004
First Named Inventor	Richard W. Foote
Art Unit	2812
Examiner Name	Not Yet Assigned
Attorney Docket Number	P05827

**U. S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
	AA	US- 4,631,803	12/30/1986	Hunter et al.	
	AB	US- 4,835,115	05/30/1989	Eklund	
	AC	US- 4,983,226	01/08/1991	Hunter et al.	
	AD	US- 5,106,777	04/21/1992	Rodder	
	AE	US- 5,358,891	10/25/1994	Tsang et al.	
	AF	US- 5,448,102	09/05/1995	Gaul et al.	
	AG	US- 5,468,676	11/21/1995	Madan	
	AH	US- 5,474,953	12/12/1995	Shimizu et al.	
	AI	US- 5,683,908	11/04/1997	Miyashita et al.	
	AJ	US- 5,872,044	02/16/1999	Hemmenway et al.	
	AK	US- 5,874,317	02/23/1999	Stolmeijer	
	AL	US- 5,920,108	07/06/1999	Hemmenway et al.	
	AM	US- 6,069,057	05/30/2000	Wu	
		US-			
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		US-			

**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)				

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SignatureDate  
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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STATEMENT BY APPLICANT**

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Sheet 2 of 2

Application Number	10/803,273
Filing Date	March 18, 2004
First Named Inventor	Richard W. Foote
Art Unit	2812
Examiner Name	Not Yet Assigned
Attorney Docket Number	P05827

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	BA	Naresh Thapar et al., "Elimination of the "Birds Beak" in Trench MOS-Gate Power Semiconductor Devices", Power Semiconductor Research Center, 1996 IEEE, Pp. 83-86.	
	BB	G. Fallico et al., "A New Process for Defect-Free Definition of Active Areas in Deep Trench Isolated Bipolar Devices", Microelectronic Engineering 15 (1991) Pp. 655-658.	
	BC	R. Bashir et al., "PLATOP: A Novel Planarized Trench Isolation and Field Oxide Formation Using Poly-Silicon", IEEE Electron Device Letters, Vol. 17, No. 7, July 1996, Pp. 352-354.	
	BD	H. Bernhard Pogge, "The Spaces Between the Functions On a Chip", Chemtech, March 1986, Pp. 168-173.	
	BE	R. Jerome et al., "The Effect of Trench Processing Conditions on Complementary Bipolar Analog Devices with SOI/Trench Isolation", IEEE 1993 Bipolar Circuits and Technology Meeting 3.2, Pp. 41-44.	
	BF		
	BG		
	BH		
	BI		
	BJ		

Examiner Signature		Date Considered	
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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